Remarks

In view of the above amendments and the following remarks, reconsideration and further examination are requested.

Claims 1, 3-5, 7 and 8 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Kawakami (US 6,332,058) in view of Siong (US 6,028,632) and Haskell (US 5,159,447).

Claims 1 and 5 have been amended so as to further distinguish the present invention from the references relied upon in the rejection.

Further, claims 1, 3-5, 7 and 8 have been amended to make a number of editorial revisions. These revisions have been made to place the claims in better U.S. form. None of these amendments have been made to narrow the scope of protection of the claims, nor to address issues related to patentability and therefore, these amendments should not be construed as limiting the scope of equivalents of the claimed features offered by the Doctrine of Equivalents.

In light of the amendments to claims 1 and 5, it is submitted that the above-mentioned rejection is no longer applicable to the claims for the following reasons.

Claim 1 is patentable over the combination of Kawakami, Siong and Haskell, since claim 1 recites a multiple decoding apparatus including, in part, a data flow controller for distributing two or more encoded data stored in a buffer for each data type and transferring the two or more encoded data in accordance with provided transfer conditions; and a decoding controller for selecting a separate buffer and a decoder, which are used for the decoding, according to a usage status of a decoder from among a plurality of separate buffers and a plurality of decoders in accordance with control information, and outputting information related to the separate buffer selected by the decoding controller, transfer conditions based on the separate buffer selected by the decoding controller, and an instruction to start decoding, respectively, to a separate buffer manager, the data flow controller, and the decoder selected by the decoding controller. The combination of Kawakami, Siong and Haskell fails to disclose or suggest the data flow controller and the decoding controller of claim 1.

Kawakami discloses an MPEG server 16 having a core 18 that receives information material (an MPEG stream) 14 and an external controller 24 operable to supply a control signal 26 to the core 18. The MPEG server 16 also includes a number of hard disk drives (HDDs) 20, DMA buffers 30, a time-divisional multiplexing controller 40, gate controllers 32, decoder

buffers 34 and decoders 22. (See column 4, line 47 – column 5, line 54 and Figures 1 and 2).

In a recordation operation, the MPEG server 16 receives the control signal 26 indicating that the MPEG server 16 is to record the information material 14. The MPEG server 16 then divides the information material 14 into a number of cells CE each having a size of four bytes. The cells CE are recorded on the HDDs 20 such that the first cell is stored on HDD 20-1, the second cell is stored on HDD 20-2, the third cell is stored on HDD 20-3, etc. Therefore, it is apparent that the information material 14 is split into a number of cells CE and the HDDs 20 are used to store the cells CE in parallel. (See column 5, line 10 – column 6, line 7).

In a reproduction operation, the MPEG server 16 receives a control signal 38 from a CPU group 36 indicating that the MPEG server 16 is to reproduce the information material 14. The cells CE stored on the HDDs 20 are read from the HDDs 20 and stored in DMA buffers 30 which respectively correspond to the HDDs 20. The cells CE are written to the DMA buffers 30 in clusters CT, which are larger than the cells CE. The controller 40 then controls the output of the information stored in the DMA buffers 30 such that desired information from each of the DMA buffers 30 is read at a desired time point. In other words, since the information material 14 is split into the cells CE which are stored on different HDDs 20 and the cells CE from each of the HDDs 20 are grouped together into the larger clusters CT when read from the HDDs 20 and stored in the respective DMA buffers 30, it is necessary to read the information from the DMA buffers 30 in an order such that the information material 14 can be properly recreated. The gate controllers 32 operate so as to allow the information output by the DMA buffers 30 under the control of the controller 40 to only be supplied to the appropriate decoder buffer 34. (See column 5, lines 34-37; column 6, lines 46-49; column 7, lines 11-16 and 55-58; and Figures 1 and 2).

Once the information material 14 is properly stored in the decoder buffer 34, it is read out from the corresponding decoder 22 as packets PT and decoded into a video signal VS and an audio signal AS. In this way, the information material 14 is reproduced. (See column 6, lines 42-59 and Figure 2).

Claim 1 of the present invention recites the data flow controller for distributing two or more encoded data stored in a buffer for each data type and transferring the two or more encoded data in accordance with provided transfer conditions. From this recitation of claim 1, it is apparent that the data flow controller distributes encoded data based on data type. It is submitted

that Kawakami fails to disclose or suggest such a feature.

Based on the above discussion of Kawakami, the information material 14 is spilt into the cells CE in 4-byte groups and stored on the HDDs 20 such that the first cell CE is stored on the HDD 20-1, the second cell CE is stored on the HDD 20-2, the third cell CE is stored on the HDD 20-3, the fourth cell CE is stored on the HDD 20-4, the fifth cell CE is stored on the HDD 20-5, the sixth cell CE is stored on the HDD 20-1, and so on until all of the information material 14 has been stored. Then, during reproduction, the cells CE are read from the HDDs 20 as the clusters CT and stored in the respective DMA buffers 30. Therefore, Kawakami distributes the data to the HDDs 20 and the DMA buffers 30 based solely on a number of bytes defined for the cells CE and the clusters CT and not on data type.

Also, in the rejection, it is indicated that the controller 40 corresponds to the claimed data flow controller. However, the controller 40 controls the output of data from the DMA buffers 30 to one of the decoder buffers 34 so that the information material 14 can be properly decoded by the decoder 22 corresponding to the decoder buffer 34. Kawakami does not disclose or suggest that the controller 40 distributes the data from the DMA buffers 30 to a number of the decoders 22 based on data type. This can be clearly seen from Figure 2 which shows each of the decoders 22 outputing both the video signal VS and the audio signal AS. Further, it is apparent that the MPEG server 16 has the plurality of buffers 34 and corresponding decoders 22 so as to reproduce a number of information materials 14 on many channels (i.e., to increase capacity) and there is no indication of distribution to the decoders 22 based on data type. (See column 5, lines 55-65). As a result, the controller 40 does not correspond to the claimed data flow controller.

Claim 1 also recites the decoding controller for selecting a separate buffer and a decoder, which are used for the decoding, according to a usage status of a decoder from among a plurality of separate buffers and a plurality of decoders in accordance with control information. Regarding this limitation, while the MPEG server 16 of Kawakami has the plurality of buffers 34 and the corresponding decoders 22 so as to reproduce a number of information materials 14 on many channels, there is no disclosure or suggestion that the controller 40 selects between the plurality of buffers 34 and the corresponding decoders 22 based on the usage status of a decoder 22. As a result, the controller 40 does not correspond to the claimed decoding controller.

Therefore, in order for the combination of Kawakami, Siong and Haskell to render claim 1 obvious, at least one of Siong and Haskell must disclose or suggest both the data flow

controller and the decoding controller recited in claim 1. However, Siong is relied upon for disclosing a separate buffer manager for controlling the outputs of a plurality of separate buffers and Haskell is relied upon as disclosing a buffer controller for a variable bit rate channel. Neither of these references discloses or suggests the data flow controller or the decoding controller of claim 1. As a result, the combination of Kawakami, Siong and Haskell fails to render claim 1 obvious.

As for claim 5, it is patentable over the combination of Kawakami, Siong and Haskell for reasons similar to those discussed above in support of claim 1. That is, claim 5 recites, in part, selecting a plurality of decoders for performing decoding and a plurality of separate buffers corresponding to the plurality of decoders, respectively, according to usage status of the plurality of decoders; and distributing two or more encoded data stored in a buffer for each data type and respectively storing the two or more encoded data in the plurality of separate buffers, which features are not disclosed or suggested by the references.

Because of the above-mentioned distinctions, it is believed clear that claims 1, 3-5, 7 and 8 are allowable over the references relied upon in the rejection. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1, 3-5, 7 and 8. Therefore, it is submitted that claims 1, 3-5, 7 and 8 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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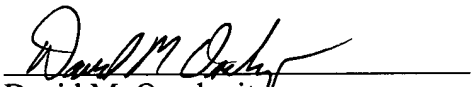
By: 

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July 13, 2005